

FORM PTO-1449  
(REV. 7-80)U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
854063.523C1APPLICATION NO.  
10/621,262INFORMATION DISCLOSURE STATEMENT  
(Use several sheets if necessary)

APPLICANTS

Nicolas Demange et al.

FILING DATE

July 15, 2003

GROUP ART UNIT

2812

## U.S. PATENT DOCUMENTS

*EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
M	AA 5,350,705	09/27/94	Brassington et al.	257	295	
	AB 5,418,388	05/23/95	Okudaira et al.	257	295	
	AC 5,519,237	05/21/96	Itoh et al.	257	306	
	AD 5,796,133	08/18/98	Kwon et al.	257	295	
	AE 5,796,136	08/18/98	Shinkawata	365	306	
	AF 5,955,758	09/21/99	Sandhu et al.	257	306	
	AG 6,028,361	02/22/00	Ooishi	257	774	
M	AH 6,063,656	05/16/00	Clampitt	438	239	
	AI					

## FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION	
				YES	NO
	AJ				
	AK				
	AL				

## OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

M	AM	Amanuma, K. et al., "Capacitor-on-Metal/Via-stacked-Plug (CMVP) Memory Cell for 0.25um CMOS Embedded Fe RAM", <i>IEEE</i> , 1998, pg. 363-366.
M	AN	Jones, Robert E. Jr., "Integration of Ferroelectric Nonvolatile Memories," <i>Solid State Technology</i> , October 1997, pp. 201-210.
M	AO	Takashima, D. et al., "A Sub-40ns Random-Access Chain FRAM Architecture with a 7ns Cell-Plate-Line Drive," <i>IEEE International Solid-State Circuits Conference</i> , 1999, pp. 102-103.
M	AP	Yamazaki, T., et al., "Advanced 0.5um FRAM Device Technology with Full Compatibility of Half-Micron CMOS Logic device", <i>Advanced Process Integration Department, Fujitsu Limited. (4 pages)</i> .

EXAMINER

H. Jay Tsa

DATE CONSIDERED

3/10/03

\* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).